WHAT IS CLAIMED IS:

1. A circuit comprising a cascaded domino four-to-two reducer.

2. The circuit of claim 1, wherein the four-to-two reducer comprises:

a first three-to-two reducer; and

a second three-to-two reducer directly connected to the first three-to-two reducer.

3. The circuit of claim 2, wherein the circuit further comprises:

a first clock input connected to the first three-to-two reducer to receive a first clock signal; and

a second clock input connected to the second three-to-two reducer to receive a second clock signal that is delayed from the first clock signal.

4. The circuit of claim 3, wherein the delay between the first clock signal and second clock signal is approximately the delay of an inverter with a fanout of 2.

5. The circuit of claim 3, wherein the four-to-two reducer includes two set-reset latches to convert the outputs of the second three-to-two reducer to static logic.

6. The circuit of claim 3, wherein the first and second three-to-two reducer both include a symmetric carry generate gate.

7. The circuit of claim 6, wherein the symmetric carry generate gates have a first evaluation block of transistors and a second evaluation block of transistors, wherein the first evaluation block and second evaluation block each have the same number of transistors.

8. The circuit of claim 7, wherein the symmetric carry generate gates have six data inputs, and wherein the gate of each of the transistors in both the first evaluation block and the second evaluation block is connected to one of the six data inputs.

9. The circuit of claim 6, wherein the first evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, wherein the second evaluation block comprises a plurality of transistors connected in a parallel relationship to each other and a plurality of transistors connected in a serial relationship to each other, and wherein the second evaluation block has the same number of transistors in said parallel relationship as the first evaluation block and the same number of transistors in said serial relationship as the first evaluation block.

10. A circuit comprising:

a first differential domino three-to-two reducer having three differential inputs and two differential outputs; and

a second differential domino three-to-two reducer having three differential inputs and two differential outputs, wherein one of the differential inputs of the second differential three-to-two reducer is connected to a differential output of the first differential three-to-two reducer, and wherein there are no static stages between the first and second differential domino three-to-two reducers.

11. The circuit of claim 10, wherein the first differential domino three-to-two reducer has an input to receive a first clock signal and the second differential domino three-to-two reducer has an input to receive a different clock signal.

12. The circuit of claim 10, wherein the first differential three-to-two reducer comprises:

a differential exclusive-OR (XOR) gate having three differential inputs and a differential output; and

a differential carry generate gate having three differential inputs and a differential output.

13. The circuit of claim 12, wherein the three differential inputs to the carry generate gate comprise three true inputs and three compliment inputs, and wherein the Miller coupling for the true inputs is equal to the Miller coupling for the compliment inputs.

14. The circuit of claim 13, wherein the differential output of the carry generate gate comprises a true output and a compliment output, and wherein the output drive strength for the true output is the same as the output drive strength for the compliment output.

15. The circuit of claim 12, wherein the load for the true inputs to the carry generate gate is the same as the load for the compliment inputs, wherein the pull down strength for the true output is the same as the pull down strength for the complement output, and wherein the pull down strength for the true inputs is the same as the pull down strength for the complement inputs.

16. A circuit comprising:

a plurality of data inputs comprising three true inputs and three compliment inputs;

a differential exclusive-OR (XOR) gate having six input ports each connected to one of said plurality of data inputs; and

a differential carry generate gate having six input ports each connected to one of said plurality of data inputs, wherein said first differential carry generate gate comprises a precharge block, a first evaluation block connected to said three true inputs, and a second evaluation block connected to said three compliment inputs, and wherein the carry generate gate is symmetric.

17. The circuit of claim 16, wherein the carry generate gate includes a first transistor connected to ground to provide a path to ground.

18. The circuit of claim 17, wherein the first evaluation block and second evaluation block each have a plurality of transistors arranged in stacks, each stack connecting said first transistor and an output of the carry generate gate, and wherein the number of transistors in each of said stacks is the same.

19. The circuit of claim 18, wherein the carry generate gate has a true output and a compliment output, wherein the three true inputs comprise a first true input, a second true input, and a third true input, wherein the three compliment inputs comprise a first compliment input, a second compliment input, and a third compliment input, and wherein the first evaluation block comprises:

a second transistor and third transistor each having a drain connected to the first transistor and a gate connected to the first true input;

a fourth transistor having a drain connected to the first transistor and a gate connected to the second true input;

a fifth transistor having a drain connected to a source of the second transistor, a gate connected to the second true input, and a drain connected to the compliment output; and

a sixth transistor having a drain connected to a source of the fourth transistor, a gate connected to the third true input, and a source connected to the compliment output.

20. The circuit of claim 19, further comprising:

a seventh transistor and eighth transistor each having a drain connected to the first transistor and a gate connected to the first compliment input;

a ninth transistor having a drain connected to the first transistor and a gate connected to the second compliment input;

a tenth transistor having a drain connected to a source of the seventh transistor, a gate connected to the second compliment input, and a drain connected to the true output; and

an eleventh transistor having a drain connected to a source of the ninth transistor, a gate connected to the third compliment input, and a source connected to the true output.

21. A method comprising:

receiving three pair of true and compliment data bits at a first differential domino three-to-two reducer;

output a first pair of true and compliment sum bits from the first three-to-two reducer to a second differential domino three-to-two reducer during the evaluation phase of a first clock;

receiving a fourth pair of true and compliment data bits at the second differential domino reducer; and

outputting a second pair of true and compliment sum bits and a pair of true and compliment carry output bits output during the evaluation phase of a second clock.

22. The method of claim 21, wherein the first pair of true and compliment sum bits are outputted directly to the second three-to-two reducer from the first three-to-two reducer.

23. The method of claim 22, wherein providing the first true and compliment sum bits to the second three-to-two reducer comprises:

outputting the first true and compliment sum bits to an exclusive-or (XOR) gate; and

outputting the first true and compliment sum bits to a symmetric carry generate gate.

24. The method of claim 21, wherein the method further comprises:

receiving the second true and compliment sum bits at a first latch;

outputting a true sum output from the first latch;

receiving the true and compliment carry output bits at a second latch; and

outputting a compliment sum output from the second latch.